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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,085	11/03/2003	Tze-chiang Chen	YOR920030586US1 (17201)	2805
23389	7590	11/30/2005	EXAMINER	
SCULLY SCOTT MURPHY & PRESSER, PC 400 GARDEN CITY PLAZA SUITE 300 GARDEN CITY, NY 11530			NGUYEN, CUONG QUANG	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/700,085	CHEN ET AL.	
	Examiner	Art Unit	
	Cuong Q. Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) 2,8-10,15-28 and 33-36 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,3-7,11-14, and 29-32 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 3, 4, 5, 11, 12 and 14 are rejected under 35 U.S.C. 102(a) as being anticipated by Bae et al. (US 6,633,066).

Regarding claims 1, 3, 4, 11, 12, Bae et al. discloses a semiconductor wafer comprising: a silicon (Si) substrate (20) (col.2 lines 36-40) performed silicon-on-insulators; a buried insulator layer (22) located on an upper surface of the substrate; an intermediate adhesion layer (18, an epitaxial silicon layer) located on an upper surface the buried insulator layer; and a Ge-containing layer (16) located on an upper surface of the intermediate adhesion layer, wherein said Ge-containing layer is attached to the buried insulator layer by the intermediate adhesion layer. Fig.4E.

It is noted that the wafer includes substrate (20), buried insulator layer (22), intermediate adhesion layer (18) and Ge-containing layer (16), so the Ge-containing layer is considered as the uppermost of the wafer. It is also noted that the intermediate

adhesion layer (18) is formed between the buried insulator layer (22) and the Ge-containing layer (16) and having the same material (epitaxial silicon) as the intermediate adhesion layer of the present invention (paragraph [0039] of the present invention's disclosure), so the intermediate adhesion layer (18) in Bae et al.'s device is capable to function as a bond between the buried insulator layer and the Ge-containing layer and is capable to eliminate Ge-oxide from the wafer as claimed.

Regarding claim 5, as shown in Bae et al.'s Fig.4E, that the substrate comprises a combination of strained and unstrained layers.

Regarding claim 14, Bae et al. teaches that the Ge-containing layer has a thickness of 80 nm (col.7 lines 31-32).

Claims 1, 3, 4, 6, 7, 11, 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Chu et al. (US 5,906,951).

Chu et al. discloses a semiconductor wafer comprising: a silicon substrate (26) performed silicon-on-insulators; a buried insulator layer (28, a non-crystalline silicon dioxide layer) located on an upper surface of the substrate; an intermediate adhesion layer (19, an epitaxial silicon layer) located on an upper surface the buried insulator layer; and a Ge-containing layer (18) located on an upper surface of the intermediate adhesion layer, wherein said Ge-containing layer is attached to the buried insulator layer by the intermediate adhesion layer. Fig.4.

It is noted that the wafer includes substrate (26), buried insulator layer (28), intermediate adhesion layer (19) and Ge-containing layer (18), so the Ge-containing

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layer is considered as the uppermost of the wafer. It is also noted that the intermediate adhesion layer (19) is formed between the buried insulator layer (28) and the Ge-containing layer (18) and having the same material (epitaxial silicon) as the intermediate adhesion layer of the present invention (paragraph [0039] of the present invention's disclosure), so the intermediate adhesion layer (18) in Chu et al.'s device is capable to function as a bond between the buried insulator layer and the Ge-containing layer and is capable to eliminate Ge-oxide from the wafer as claimed.

Claims 1, 3, 4, 6, 7, 11, 12, 13 and 29-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Fitzgerald (US 6,677,655).

Regarding claims 1, 3, 4, 6, 7, 11, 12, 13, Fitzgerald discloses a semiconductor wafer comprising: a silicon substrate (308) performed silicon-on-insulators; a buried insulator layer (310, a non-crystalline silicon dioxide layer) located on an upper surface of the substrate; an intermediate adhesion layer (306, an epitaxial silicon layer) located on an upper surface the buried insulator layer; and a pure Ge layer (302) located on an upper surface of the intermediate adhesion layer, wherein said Ge-containing layer is attached to the buried insulator layer by the intermediate adhesion layer. Fig.3D.

It is noted that the wafer includes substrate (308), buried insulator layer (310), intermediate adhesion layer (306) and Ge-containing layer (302), so the Ge-containing layer is considered as the uppermost of the wafer. It is also noted that the intermediate adhesion layer (306) is formed between the buried insulator layer (310) and the Ge-containing layer (302) and having the same material (epitaxial silicon) as the

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intermediate adhesion layer of the present invention (paragraph [0039] of the present invention's disclosure), so the intermediate adhesion layer (306) in Fitzgerald's device is capable to function as a bond between the buried insulator layer and the Ge-containing layer and is capable to eliminate Ge-oxide from the wafer as claimed.

Regarding claims 29-32, Fitzgerald teach that a monolithic optoelectronic integrated circuit including a si-containing circuit is formed on the semiconductor wafer (col.1 lines 9-23) lemst one device or circuit located thereon. Fitzgerald further teaches that the device is a Ge-photodetector (col.7 lines 30-40).

Response to Arguments

2. Applicant's arguments filed 11-04-05 have been fully considered but they are not persuasive as above discussion.

Conclusion

3. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571)

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272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

4. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Eddie Lee who can be reached on (571) 272-1732.

5. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

A handwritten signature in black ink, appearing to read 'Cuong Nguyen', with a long vertical line extending downwards from the end of the signature.

Cuong Nguyen

Primary examiner

11/23/05